

| Absolute Maximum Ratings (Notes 1 \& 2) |  |  |  |
| :---: | :---: | :---: | :---: |
| If Military/Aerospace specified | devices are required, | Storage Temperature Range | $-65^{\circ} \mathrm{C}$ to $+150^{\circ} \mathrm{C}$ |
| please contact the National | emiconductor Sales | Package Dissipation at $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | 875 mW |
| Office/Distributors for availability | and specifications. | ESD Susceptibility (Note 10) | 800 V |
| Supply Voltage ( $\mathrm{V}_{\mathrm{CC}}$ ) (Note 3) | 6.5 V |  |  |
| Voltage |  | Operating Ratings (Notes 1 \& 2) |  |
| Logic Control Inputs | $-0.3 \mathrm{~V} \text { to }+18 \mathrm{~V}$ |  |  |
| At Other Input and Outputs Lead Temp. (Soldering, 10 seconds) | -0.3 V to $\left(\mathrm{V}_{\mathrm{Cc}}+0.3 \mathrm{~V}\right)$ | ADC0801/02LJ, ADC0802LJ/883 | $\mathrm{MINS}^{\text {m }}$, $\mathrm{T}_{\text {A }} \leq \mathrm{T}_{\text {MAX }}$ $-55^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+125^{\circ} \mathrm{C}$ |
| Dual-In-Line Package (plastic) | $260^{\circ} \mathrm{C}$ | ADC0801/02/03/04LCJ | $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+85^{\circ} \mathrm{C}$ |
| Dual-In-Line Package (ceramic) | $300^{\circ} \mathrm{C}$ | ADC0801/02/03/05LCN | $-40^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+85^{\circ} \mathrm{C}$ |
| Surface Mount Package |  | ADC0804LCN | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+70^{\circ} \mathrm{C}$ |
| Vapor Phase (60 seconds) | $215^{\circ} \mathrm{C}$ | ADC0802/03/04LCV | $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+70^{\circ} \mathrm{C}$ |
| Infrared (15 seconds) | $220^{\circ} \mathrm{C}$ | ADC0802/03/04LCWM Range of $\mathrm{V}_{C C}$ | 4.5 V VC to 6.3 V VC |

## Electrical Characteristics

The following specifications apply for $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\mathrm{DC}}, \mathrm{T}_{\mathrm{MIN}} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\mathrm{MAX}}$ and $\mathrm{f}_{C L K}=640 \mathrm{kHz}$ unless otherwise specified.

| Parameter | Conditions | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: |
| ADC0801: Total Adjusted Error (Note 8) | With Full-Scale Adj. (See Section 2.5.2) |  |  | $\pm 1 / 4$ | LSB |
| ADC0802: Total Unadjusted Error (Note 8) | $\mathrm{V}_{\text {REF }} / 2=2.500 \mathrm{~V}_{\mathrm{DC}}$ |  |  | $\pm 1 / 2$ | LSB |
| ADC0803: Total Adjusted Error (Note 8) | With Full-Scale Adj. (See Section 2.5.2) |  |  | $\pm 1 / 2$ | LSB |
| ADC0804: Total Unadjusted Error (Note 8) | $\mathrm{V}_{\text {REF }} / 2=2.500 \mathrm{~V}_{\mathrm{DC}}$ |  |  | $\pm 1$ | LSB |
| ADC0805: Total Unadjusted Error (Note 8) | $\mathrm{V}_{\text {REF }} / 2-\mathrm{No}$ Connection |  |  | $\pm 1$ | LSB |
| $\mathrm{V}_{\text {REF }} / 2$ Input Resistance (Pin 9) | $\begin{aligned} & \text { ADC0801/02/03/05 } \\ & \text { ADC0804 (Note 9) } \\ & \hline \end{aligned}$ | $\begin{gathered} \hline 2.5 \\ 0.75 \\ \hline \end{gathered}$ | $\begin{aligned} & 8.0 \\ & 1.1 \\ & \hline \end{aligned}$ |  | $\begin{aligned} & \mathrm{k} \Omega \\ & \mathrm{k} \Omega \\ & \hline \end{aligned}$ |
| Analog Input Voltage Range | (Note 4) V(+) or V(-) | Gnd-0.05 |  | $\mathrm{V}_{\mathrm{CC}}+0.05$ | $\mathrm{V}_{\mathrm{DC}}$ |
| DC Common-Mode Error | Over Analog Input Voltage Range |  | $\pm 1 / 16$ | $\pm 1 / 8$ | LSB |
| Power Supply Sensitivity | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\mathrm{DC}} \pm 10 \% \text { Over } \\ & \text { Allowed } \mathrm{V}_{\text {IN }}(+) \text { and } \mathrm{V}_{\mathrm{IN}}(-) \\ & \text { Voltage Range (Note 4) } \end{aligned}$ |  | $\pm 1 / 16$ | $\pm 1 / 8$ | LSB |

## AC Electrical Characteristics

The following specifications apply for $\mathrm{V}_{C C}=5 \mathrm{~V}_{\mathrm{DC}}$ and $\mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| $\mathrm{T}_{\mathrm{C}}$ | Conversion Time | $\mathrm{f}_{\mathrm{CLK}}=640 \mathrm{kHz}$ (Note 6) | 103 |  | 114 | $\mu \mathrm{s}$ |
| $\mathrm{T}_{\mathrm{C}}$ | Conversion Time | (Note 5, 6) | 66 |  | 73 | 1/fCLK |
| ${ }_{\text {f CLK }}$ | Clock Frequency Clock Duty Cycle | $\begin{aligned} & \mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V},(\text { Note } 5) \\ & \text { (Note 5) } \end{aligned}$ | $\begin{gathered} 100 \\ 40 \end{gathered}$ | 640 | $\begin{gathered} 1460 \\ 60 \end{gathered}$ | $\begin{gathered} \hline \mathrm{kHz} \\ \% \end{gathered}$ |
| CR | Conversion Rate in Free-Running Mode | $\overline{\text { INTR }}$ tied to $\overline{\text { WR }}$ with $\overline{\mathrm{CS}}=0 \mathrm{~V}_{\mathrm{DC}}, \mathrm{f}_{\mathrm{CLK}}=640 \mathrm{kHz}$ | 8770 |  | 9708 | conv/s |
| $t_{W}(\overline{W R})$ L | Width of WR Input (Start Pulse Width) | $\overline{\mathrm{CS}}=0 \mathrm{~V}_{\mathrm{DC}}$ (Note 7) | 100 |  |  | ns |
| ${ }^{\text {taCC }}$ | Access Time (Delay from Falling Edge of RD to Output Data Valid) | $\mathrm{C}_{\mathrm{L}}=100 \mathrm{pF}$ |  | 135 | 200 | ns |
| $\mathrm{t}_{1 \mathrm{H},}, \mathrm{t}_{\mathrm{OH}}$ | TRI-STATE Control (Delay from Rising Edge of RD to Hi-Z State) | $\mathrm{C}_{\mathrm{L}}=10 \mathrm{pF}, \mathrm{R}_{\mathrm{L}}=10 \mathrm{k}$ <br> (See TRI-STATE Test Circuits) |  | 125 | 200 | ns |
| ${ }_{\text {t }}^{\text {W }}$, $\mathrm{t}_{\text {RI }}$ | Delay from Falling Edge of $\overline{\mathrm{WR}}$ or $\overline{\mathrm{RD}}$ to Reset of $\overline{\mathrm{INTR}}$ |  |  | 300 | 450 | ns |
| $\mathrm{C}_{\text {IN }}$ | Input Capacitance of Logic Control Inputs |  |  | 5 | 7.5 | pF |
| COUT | TRI-STATE Output Capacitance (Data Buffers) |  |  | 5 | 7.5 | pF |
| CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately] |  |  |  |  |  |  |
| $\mathrm{V}_{\text {IN }}(1)$ | Logical "1" Input Voltage (Except Pin 4 CLK IN) | $\mathrm{V}_{\mathrm{CC}}=5.25 \mathrm{~V}_{\mathrm{DC}}$ | 2.0 |  | 15 | $\mathrm{V}_{\mathrm{DC}}$ |

AC Electrical Characteristics (Continued)
The following specifications apply for $\mathrm{V}_{\mathrm{CC}}=5 \mathrm{~V}_{\mathrm{DC}}$ and $\mathrm{T}_{\text {MIN }} \leq \mathrm{T}_{\mathrm{A}} \leq \mathrm{T}_{\mathrm{MAX}}$, unless otherwise specified.

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| CONTROL INPUTS [Note: CLK IN (Pin 4) is the input of a Schmitt trigger circuit and is therefore specified separately] |  |  |  |  |  |  |
| $\mathrm{V}_{\text {IN }}(0)$ | Logical " 0 " Input Voltage (Except Pin 4 CLK IN) | $\mathrm{V}_{\mathrm{CC}}=4.75 \mathrm{~V}_{\mathrm{DC}}$ |  |  | 0.8 | $\mathrm{V}_{\mathrm{DC}}$ |
| $\mathrm{I}_{\text {IN }}(1)$ | Logical "1" Input Current (All Inputs) | $\mathrm{V}_{\mathrm{IN}}=5 \mathrm{~V}_{\mathrm{DC}}$ |  | 0.005 | 1 | $\mu A_{D C}$ |
| IIN (0) | Logical " 0 " Input Current (All Inputs) | $\mathrm{V}_{\mathrm{IN}}=0 \mathrm{~V}_{\mathrm{DC}}$ | -1 | -0.005 |  | $\mu A_{D C}$ |
| CLOCK IN AND CLOCK R |  |  |  |  |  |  |
| $\mathrm{V}_{\mathrm{T}}+$ | CLK IN (Pin 4) Positive Going Threshold Voltage |  | 2.7 | 3.1 | 3.5 | $\mathrm{V}_{\mathrm{DC}}$ |
| $\mathrm{V}_{\mathrm{T}}-$ | CLK IN (Pin 4) Negative Going Threshold Voltage |  | 1.5 | 1.8 | 2.1 | $\mathrm{V}_{\mathrm{DC}}$ |
| $\mathrm{V}_{\mathrm{H}}$ | CLK IN (Pin 4) Hysteresis $\left(\mathrm{V}_{\mathrm{T}}+\right)-\left(\mathrm{V}_{\mathrm{T}}-\right)$ |  | 0.6 | 1.3 | 2.0 | $\mathrm{V}_{\mathrm{DC}}$ |
| $\mathrm{V}_{\text {OUT }}(0)$ | Logical "0" CLK R Output Voltage | $\begin{aligned} & \mathrm{I}_{\mathrm{O}}=360 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{CC}}=4.75 \mathrm{~V}_{\mathrm{DC}} \end{aligned}$ |  |  | 0.4 | $\mathrm{V}_{\mathrm{DC}}$ |
| $V_{\text {OUT }}(1)$ | Logical " 1 " CLK R Output Voltage | $\begin{aligned} & \mathrm{I}_{\mathrm{O}}=-360 \mu \mathrm{~A} \\ & \mathrm{~V}_{\mathrm{CC}}=4.75 \mathrm{~V}_{\mathrm{DC}} \end{aligned}$ | 2.4 |  |  | $\mathrm{V}_{\mathrm{DC}}$ |
| DATA OUTPUTS AND INTR |  |  |  |  |  |  |
| $\mathrm{V}_{\text {OUT }}(0)$ | Logical " 0 " Output Voltage <br> Data Outputs <br> INTR Output | $\begin{aligned} & \mathrm{I}_{\mathrm{OUT}}=1.6 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=4.75 \mathrm{~V}_{\mathrm{DC}} \\ & \mathrm{I}_{\mathrm{OUT}}=1.0 \mathrm{~mA}, \mathrm{~V}_{\mathrm{CC}}=4.75 \mathrm{~V}_{\mathrm{DC}} \end{aligned}$ |  |  | $\begin{aligned} & 0.4 \\ & 0.4 \end{aligned}$ | $V_{D C}$ <br> $V_{D C}$ |
| $\mathrm{V}_{\text {OUT }}(1)$ | Logical "1" Output Voltage | $\mathrm{I}_{\mathrm{O}}=-360 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{CC}}=4.75 \mathrm{~V}_{\mathrm{DC}}$ | 2.4 |  |  | $V_{D C}$ |
| $\mathrm{V}_{\text {OUT }}(1)$ | Logical "1" Output Voltage | $\mathrm{I}_{\mathrm{O}}=-10 \mu \mathrm{~A}, \mathrm{~V}_{\mathrm{CC}}=4.75 \mathrm{~V}_{\mathrm{DC}}$ | 4.5 |  |  | $V_{D C}$ |
| Iout | TRI-STATE Disabled Output Leakage (All Data Buffers) | $\begin{aligned} & \mathrm{V}_{\text {OUT }}=0 \mathrm{~V}_{\mathrm{DC}} \\ & \mathrm{~V}_{\text {OUT }}=5 \mathrm{~V}_{\mathrm{DC}} \end{aligned}$ | -3 |  | 3 | $\mu A_{D C}$ <br> $\mu A_{D C}$ |
| Isource |  | $\mathrm{V}_{\text {OUT }}$ Short to Gnd, $\mathrm{T}_{\text {A }}=25^{\circ} \mathrm{C}$ | 4.5 | 6 |  | $m A_{D C}$ |
| ISINK |  | $\mathrm{V}_{\text {OUT }}$ Short to $\mathrm{V}_{\mathrm{CC}}, \mathrm{T}_{\mathrm{A}}=25^{\circ} \mathrm{C}$ | 9.0 | 16 |  | $m A_{D C}$ |
| POWER SUPPLY |  |  |  |  |  |  |
| $I_{\text {cc }}$ | Supply Current (Includes Ladder Current) <br> ADC0801/02/03/04LCJ/05 ADC0804LCN/LCV/LCWM | $\begin{aligned} & \mathrm{f}_{\mathrm{CLK}}=640 \mathrm{kHz}, \\ & \mathrm{~V}_{\mathrm{REF}} / 2=\mathrm{NC}, \mathrm{~T}_{\mathrm{A}}=25^{\circ} \mathrm{C} \\ & \text { and } \overline{\mathrm{CS}}=5 \mathrm{~V} \end{aligned}$ |  | $\begin{aligned} & 1.1 \\ & 1.9 \end{aligned}$ | $\begin{aligned} & 1.8 \\ & 2.5 \end{aligned}$ | $\begin{aligned} & \mathrm{mA} \\ & \mathrm{~mA} \end{aligned}$ |

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.
Note 2: All voltages are measured with respect to Gnd, unless otherwise specified. The separate A Gnd point should always be wired to the D Gnd.
Note 3: A zener diode exists, internally, from $V_{C C}$ to $G$ nd and has a typical breakdown voltage of $7 \mathrm{~V}_{\mathrm{DC}}$
Note 4: For $\mathrm{V}_{I N}(-) \geq \mathrm{V}_{I N}(+)$ the digital output code will be 00000000 . Two on-chip diodes are tied to each analog input (see block diagram) which will forward conduct for analog input voltages one diode drop below ground or one diode drop greater than the $\mathrm{V}_{\mathrm{CC}}$ supply. Be careful, during testing at low $\mathrm{V}_{\mathrm{CC}}$ levels ( 4.5 V ), as high level analog inputs ( 5 V ) can cause this input diode to conduct-especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog $\mathrm{V}_{\mathrm{IN}}$ does not exceed the supply voltage by more than 50 mV , the output code will be correct. To achieve an absolute $0 \mathrm{~V}_{\mathrm{DC}}$ to $5 \mathrm{~V}_{\mathrm{DC}}$ input voltage range will therefore require a minimum supply voltage of $4.950 \mathrm{~V}_{\mathrm{DC}}$ over temperature variations, initial tolerance and loading.
Note 5: Accuracy is guaranteed at $\mathrm{f}_{\text {CLK }}=640 \mathrm{kHz}$. At higher clock frequencies accuracy can degrade. For lower clock frequencies, the duty cycle limits can be extended so long as the minimum clock high time interval or minimum clock low time interval is no less than 275 ns.
Note 6: With an asynchronous start pulse, up to 8 clock periods may be required before the internal clock phases are proper to start the conversion process. The start request is internally latched, see Figure 2 and section 2.0.
Note 7: The $\overline{\mathrm{CS}}$ input is assumed to bracket the $\overline{\mathrm{WR}}$ strobe input and therefore timing is dependent on the $\overline{\mathrm{WR}}$ pulse width. An arbitrarily wide pulse width will hold the converter in a reset mode and the start of conversion is initiated by the low to high transition of the $\overline{W R}$ pulse (see timing diagrams).
Note 8: None of these A/Ds requires a zero adjust (see section 2.5.1). To obtain zero code at other analog input voltages see section 2.5 and Figure 5
Note 9: The $\mathrm{V}_{\text {REF }} / 2$ pin is the center point of a two-resistor divider connected from $\mathrm{V}_{\mathrm{CC}}$ to ground. In all versions of the ADC0801, ADC0802, ADC0803, and ADC0805, and in the ADC0804LCJ, each resistor is typically $16 \mathrm{k} \Omega$. In all versions of the ADC0804 except the ADC0804LCJ, each resistor is typically $2.2 \mathrm{k} \Omega$. Note 10: Human body model, 100 pF discharged through a $1.5 \mathrm{k} \Omega$ resistor.


## TRI-STATE Test Circuits and Waveforms



Timing Diagrams (All timing is measured from the $50 \%$ voltage points)


Note: Read strobe must occur 8 clock periods ( $8 / \mathrm{f}_{\mathrm{CLK}}$ ) after assertion of interrupt to guarantee reset of $\overline{\mathrm{NTR}}$.
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Output Buffers with A/D Data Enabled

*A/D output data is updated 1 CLK period prior to assertion of $\overline{\text { INTR }}$

Increasing Bus Drive and/or Reducing Time on Bus

*Allows output data to set-up at falling edge of $\overline{\mathrm{CS}}$

Typical Applications (Continued)


Note 1: Oversample whenever possible [keep fs $>2 f(-60)$ ] to eliminate input frequency folding (aliasing) and to allow for the skirt response of the filter.
Note 2: Consider the amplitude errors which are introduced within the passband of the filter.

70\% Power Savings by Clock Gating


Power Savings by A/D and $V_{\text {REF }}$ Shutdown

*Use ADC0801, 02, 03 or 05 for lowest power consumption.
Note: Logic inputs can be driven to $\mathrm{V}_{\mathrm{CC}}$ with $\mathrm{A} / \mathrm{D}$ supply at zero volts.
Buffer prevents data bus from overdriving output of A/D when in shutdown mode.

## Functional Description

### 1.0 UNDERSTANDING A/D ERROR SPECS

A perfect A/D transfer characteristic (staircase waveform) is shown in Figure 1a. The horizontal scale is analog input voltage and the particular points labeled are in steps of 1 LSB ( 19.53 mV with 2.5 V tied to the $\mathrm{V}_{\mathrm{REF}} / 2 \mathrm{pin}$ ). The digital output codes that correspond to these inputs are shown as $D-1, D$, and $D+1$. For the perfect $A / D$, not only will centervalue ( $A-1, A, A+1, \ldots$. ) analog inputs produce the correct output ditigal codes, but also each riser (the transitions between adjacent output codes) will be located $\pm 1 / 2$ LSB away from each center-value. As shown, the risers are ideal and have no width. Correct digital output codes will be provided for a range of analog input voltages that extend $\pm 1 / 2$ LSB from the ideal center-values. Each tread (the range of analog input voltage that provides the same digital output code) is therefore 1 LSB wide.
Figure 16 shows a worst case error plot for the ADC0801. All center-valued inputs are guaranteed to produce the correct output codes and the adjacent risers are guaranteed to be no closer to the center-value points than $\pm 1 / 4 \mathrm{LSB}$. In

other words, if we apply an analog input equal to the centervalue $\pm 1 / 4$ LSB, we guarantee that the A/D will produce the correct digital code. The maximum range of the position of the code transition is indicated by the horizontal arrow and it is guaranteed to be no more than $1 / 2$ LSB.
The error curve of Figure $1 c$ shows a worst case error plot for the ADC0802. Here we guarantee that if we apply an analog input equal to the LSB analog voltage center-value the A/D will produce the correct digital code.
Next to each transfer function is shown the corresponding error plot. Many people may be more familiar with error plots than transfer functions. The analog input voltage to the A/D is provided by either a linear ramp or by the discrete output steps of a high resolution DAC. Notice that the error is continuously displayed and includes the quantization uncertainty of the A/D. For example the error at point 1 of Figure 1a is $+1 / 2$ LSB because the digital code appeared $1 / 2$ LSB in advance of the center-value of the tread. The error plots always have a constant negative slope and the abrupt upside steps are always 1 LSB in magnitude.
a) Accuracy $= \pm 0$ LSB: A Perfect A/D


b) Accuracy $= \pm 1 / 4$ LSB



Error Plot
c) Accuracy $= \pm 1 / 2$ LSB

FIGURE 1. Clarifying the Error Specs of an A/D Converter

## Functional Description (Continued)

### 2.0 FUNCTIONAL DESCRIPTION

The ADC0801 series contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage $\left[\mathrm{V}_{I N}(+)-\mathrm{V}_{\mathrm{IN}}(-)\right]$ to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons ( 64 clock cycles) a digital 8 -bit binary code (1111 $1111=$ full-scale) is transferred to an output latch and then an interrupt is asserted (INTR makes a high-to-low transition). A conversion in process can be interrupted by issuing a second start command. The device may be operated in the free-running mode by connecting INTR to the $\overline{\mathrm{WR}}$ input with $\overline{\mathrm{CS}}=0$. To ensure start-up under all possible conditions, an external $\overline{\mathrm{WR}}$ pulse is required during the first power-up cycle.
On the high-to-low transition of the $\overline{W R}$ input the internal SAR latches and the shift register stages are reset. As long as the $\overline{C S}$ input and $\overline{W R}$ input remain low, the A/D will remain in a reset state. Conversion will start from 1 to 8 clock periods after at least one of these inputs makes a low-tohigh transition.

A functional diagram of the A/D converter is shown in Figure 2. All of the package pinouts are shown and the major logic control paths are drawn in heavier weight lines.
The converter is started by having $\overline{\mathrm{CS}}$ and $\overline{\mathrm{WR}}$ simultaneously low. This sets the start flip-flop (F/F) and the resulting " 1 " level resets the 8 -bit shift register, resets the Interrupt (INTR) F/F and inputs a " 1 " to the D flop, F/F1, which is at the input end of the 8 -bit shift register. Internal clock signals then transfer this " 1 " to the Q output of F/F1. The AND gate, G1, combines this "1" output with a clock signal to provide a reset signal to the start $F / F$. If the set signal is no longer present (either $\overline{W R}$ or $\overline{C S}$ is a " 1 ") the start $F / F$ is reset and the 8 -bit shift register then can have the " 1 " clocked in, which starts the conversion process. If the set signal were to still be present, this reset pulse would have no effect (both outputs of the start F/F would momentarily be at a "1" level) and the 8 -bit shift register would continue to be held in the reset mode. This logic therefore allows for wide $\overline{\mathrm{CS}}$ and $\overline{\mathrm{WR}}$ signals and the converter will start after at least one of these signals returns high and the internal clocks again provide a reset signal for the start F/F.


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Note 1: $\overline{\mathrm{CS}}$ shown twice for clarity.
Note 2: SAR = Successive Approximation Register.
FIGURE 2. Block Diagram

## Functional Description (Continued)

After the " 1 " is clocked through the 8 -bit shift register (which completes the SAR search) it appears as the input to the D-type latch, LATCH 1. As soon as this " 1 " is output from the shift register, the AND gate, G2, causes the new digital word to transfer to the TRI-STATE output latches. When LATCH 1 is subsequently enabled, the $Q$ output makes a high-to-low transition which causes the INTR F/F to set. An inverting buffer then supplies the INTR input signal.
Note that this $\overline{\text { SET }}$ control of the INTR F/F remains low for 8 of the external clock periods (as the internal clocks run at $1 / 8$ of the frequency of the external clock). If the data output is continuously enabled ( $\overline{\mathrm{CS}}$ and $\overline{\mathrm{RD}}$ both held low), the INTR output will still signal the end of conversion (by a high-to-low transition), because the SET input can control the Q output of the INTR F/F even though the RESET input is constantly at a " 1 " level in this operating mode. This INTR output will therefore stay low for the duration of the $\overline{\mathrm{SET}}$ signal, which is 8 periods of the external clock frequency (assuming the A/D is not started during this interval).
When operating in the free-running or continuous conversion mode ( $\overline{\mathrm{NTR}}$ pin tied to $\overline{\mathrm{WR}}$ and $\overline{\mathrm{CS}}$ wired low-see also section 2.8), the START F/F is SET by the high-to-low transition of the INTR signal. This resets the SHIFT REGISTER which causes the input to the D-type latch, LATCH 1, to go low. As the latch enable input is still present, the $\bar{Q}$ output will go high, which then allows the INTR F/F to be RESET. This reduces the width of the resulting $\overline{\text { NTR }}$ output pulse to only a few propagation delays (approximately 300 ns).
When data is to be read, the combination of both $\overline{C S}$ and $\overline{R D}$ being low will cause the INTR F/F to be reset and the TRI-STATE output latches will be enabled to provide the 8bit digital outputs.

### 2.1 Digital Control Inputs

The digital control inputs ( $\overline{\mathrm{CS}}, \overline{\mathrm{RD}}$, and $\overline{\mathrm{WR}}$ ) meet standard T2L logic voltage levels. These signals have been renamed when compared to the standard A/D Start and Output Enable labels. In addition, these inputs are active low to allow an easy interface to microprocessor control busses. For non-microprocessor based applications, the $\overline{\mathrm{CS}}$ input (pin 1) can be grounded and the standard A/D Start function is obtained by an active low pulse applied at the WR input (pin 3) and the Output Enable function is caused by an active low pulse at the $\overline{\mathrm{RD}}$ input (pin 2).

### 2.2 Analog Differential Voltage Inputs and <br> Common-Mode Rejection

This A/D has additional applications flexibility due to the analog differential voltage input. The $\mathrm{V}_{\mathrm{IN}}(-)$ input (pin 7) can be used to automatically subtract a fixed voltage value from the input reading (tare correction). This is also useful in $4 \mathrm{~mA}-20 \mathrm{~mA}$ current loop conversion. In addition, commonmode noise can be reduced by use of the differential input. The time interval between sampling $\mathrm{V}_{\mathrm{IN}}(+)$ and $\mathrm{V}_{\mathrm{IN}}(-)$ is 4$1 / 2$ clock periods. The maximum error voltage due to this
slight time difference between the input voltage samples is given by:

$$
\Delta \mathrm{V}_{\mathrm{e}}(\mathrm{MAX})=\left(\mathrm{V}_{\mathrm{P}}\right)\left(2 \pi \mathrm{f}_{\mathrm{cm}}\right)\left(\frac{4.5}{\mathrm{f}_{\mathrm{CLK}}}\right)
$$

where:
$\Delta V_{e}$ is the error voltage due to sampling delay
$V_{P}$ is the peak value of the common-mode voltage
$f_{\mathrm{cm}}$ is the common-mode frequency
As an example, to keep this error to $1 / 4 \mathrm{LSB}(\sim 5 \mathrm{mV})$ when operating with a 60 Hz common-mode frequency, $\mathrm{f}_{\mathrm{cm}}$, and using a 640 kHz A/D clock, $\mathrm{f}_{\mathrm{CLK}}$, would allow a peak value of the common-mode voltage, $\mathrm{V}_{\mathrm{P}}$, which is given by:

$$
\mathrm{V}_{\mathrm{P}}=\frac{\left[\Delta \mathrm{V}_{\mathrm{e}(\mathrm{MAX})}\left(\mathrm{f}_{\mathrm{CLK}}\right)\right]}{\left(2 \pi \mathrm{f}_{\mathrm{cm}}\right)(4.5)}
$$

or

$$
V_{P}=\frac{\left(5 \times 10^{-3}\right)\left(640 \times 10^{3}\right)}{(6.28)(60)(4.5)}
$$

which gives
$\mathrm{V}_{\mathrm{P}} \cong 1.9 \mathrm{~V}$.
The allowed range of analog input voltages usually places more severe restrictions on input common-mode noise levels.
An analog input voltage with a reduced span and a relatively large zero offset can be handled easily by making use of the differential input (see section 2.4 Reference Voltage).

### 2.3 Analog Inputs

2.3.1 Input Current

## Normal Mode

Due to the internal switching action, displacement currents will flow at the analog inputs. This is due to on-chip stray capacitance to ground as shown in Figure 3.


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ron of SW 1 and $S W 2 \cong 5 \mathrm{k} \Omega$
$\mathrm{r}=\mathrm{rON} \mathrm{C}_{\text {STRAY }} \cong 5 \mathrm{k} \Omega \times 12 \mathrm{pF}=60 \mathrm{~ns}$
FIGURE 3. Analog Input Impedance

## Functional Description (Continued)

The voltage on this capacitance is switched and will result in currents entering the $\mathrm{V}_{I N}(+)$ input pin and leaving the $\mathrm{V}_{\mathrm{IN}}(-)$ input which will depend on the analog differential input voltage levels. These current transients occur at the leading edge of the internal clocks. They rapidly decay and do not cause errors as the on-chip comparator is strobed at the end of the clock period.

## Fault Mode

If the voltage source applied to the $\mathrm{V}_{\mathrm{IN}}(+)$ or $\mathrm{V}_{\mathrm{IN}}(-)$ pin exceeds the allowed operating range of $\mathrm{V}_{\mathrm{CC}}+50 \mathrm{mV}$, large input currents can flow through a parasitic diode to the $\mathrm{V}_{\mathrm{CC}}$ pin. If these currents can exceed the 1 mA max allowed spec, an external diode (1N914) should be added to bypass this current to the $\mathrm{V}_{\mathrm{CC}}$ pin (with the current bypassed with this diode, the voltage at the $\mathrm{V}_{\mathrm{IN}}(+)$ pin can exceed the $\mathrm{V}_{\mathrm{CC}}$ voltage by the forward voltage of this diode).

### 2.3.2 Input Bypass Capacitors

Bypass capacitors at the inputs will average these charges and cause a DC current to flow through the output resistances of the analog signal sources. This charge pumping action is worse for continuous conversions with the $\mathrm{V}_{\mathrm{IN}}(+)$ input voltage at full-scale. For continuous conversions with a 640 kHz clock frequency with the $\mathrm{V}_{\mathrm{IN}}(+)$ input at 5 V , this DC current is at a maximum of approximately $5 \mu \mathrm{~A}$. Therefore, bypass capacitors should not be used at the analog inputs or the $V_{\text {REF }} / 2$ pin for high resistance sources ( $>1$ $\mathrm{k} \Omega$ ). If input bypass capacitors are necessary for noise filtering and high source resistance is desirable to minimize capacitor size, the detrimental effects of the voltage drop across this input resistance, which is due to the average value of the input current, can be eliminated with a full-scale adjustment while the given source resistor and input bypass capacitor are both in place. This is possible because the average value of the input current is a precise linear function of the differential input voltage.

### 2.3.3 Input Source Resistance

Large values of source resistance where an input bypass capacitor is not used, will not cause errors as the input currents settle out prior to the comparison time. If a low pass filter is required in the system, use a low valued series resistor ( $\leq 1 \mathrm{k} \Omega$ ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, ( $\leq 1 \mathrm{k} \Omega$ ), a $0.1 \mu \mathrm{~F}$ bypass capacitor at the inputs will prevent noise pickup due to series lead inductance of a long wire. A $100 \Omega$ series resistor can be used to isolate this ca-pacitor-both the R and C are placed outside the feedback loop-from the output of an op amp, if used.

### 2.3.4 Noise

The leads to the analog inputs (pin 6 and 7) should be kept as short as possible to minimize input noise coupling. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should, in general, be kept below $5 \mathrm{k} \Omega$. Larger values of source resistance can cause undesired system noise pickup. Input bypass capacitors, placed from the analog inputs to ground, will eliminate system noise pickup but can create analog scale errors as these capacitors will average the transient input switching currents of the A/D (see section 2.3.1.). This scale error depends on both a large source
resistance and the use of an input bypass capacitor. This error can be eliminated by doing a full-scale adjustment of the $A / D$ (adjust $V_{\text {REF }} / 2$ for a proper full-scale reading-see section 2.5.2 on Full-Scale Adjustment) with the source resistance and input bypass capacitor in place.

### 2.4 Reference Voltage

2.4.1 Span Adjust

For maximum applications flexibility, these $A / D s$ have been designed to accommodate a $5 \mathrm{~V}_{\mathrm{DC}}, 2.5 \mathrm{~V}_{\mathrm{DC}}$ or an adjusted voltage reference. This has been achieved in the design of the IC as shown in Figure 4.


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FIGURE 4. The Veference Design on the IC
Notice that the reference voltage for the IC is either $1 / 2$ of the voltage applied to the $\mathrm{V}_{\mathrm{CC}}$ supply pin, or is equal to the voltage that is externally forced at the $\mathrm{V}_{\text {REF }} / 2$ pin. This allows for a ratiometric voltage reference using the $\mathrm{V}_{\mathrm{CC}}$ supply, a $5 \mathrm{~V}_{\mathrm{DC}}$ reference voltage can be used for the $\mathrm{V}_{\mathrm{CC}}$ supply or a voltage less than $2.5 \mathrm{~V}_{\mathrm{DC}}$ can be applied to the $\mathrm{V}_{\text {REF }} / 2$ input for increased application flexibility. The internal gain to the $\mathrm{V}_{\text {REF }} / 2$ input is 2 , making the full-scale differential input voltage twice the voltage at pin 9.
An example of the use of an adjusted reference voltage is to accommodate a reduced span-or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from $0.5 \mathrm{~V}_{\mathrm{DC}}$ to $3.5 \mathrm{~V}_{\mathrm{DC}}$, instead of 0 V to $5 \mathrm{~V}_{\mathrm{DC}}$, the span would be 3 V as shown in Figure 5. With $0.5 \mathrm{~V}_{\mathrm{DC}}$ applied to the $\mathrm{V}_{\mathrm{IN}}(-)$ pin to absorb the offset, the reference voltage can be made equal to $1 / 2$ of the 3 V span or $1.5 \mathrm{~V}_{\mathrm{DC}}$. The A/D now will encode the $\mathrm{V}_{\mathrm{IN}}(+)$ signal from 0.5 V to 3.5 V with the 0.5 V input corresponding to zero and the $3.5 \mathrm{~V}_{\mathrm{DC}}$ input corresponding to full-scale. The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

## Functional Description (Continued)



## a) Analog Input Signal Example

b) Accommodating an Analog Input from 0.5 V (Digital Out $==00_{\text {HEX }}$ ) to 3.5 V (Digital Out $=$ FF FHEX $^{\text {) }}$

## FIGURE 5. Adapting the A/D Analog Input Voltages to Match an Arbitrary Input Signal Range

### 2.4.2 Reference Accuracy Requirements

The converter can be operated in a ratiometric mode or an absolute mode. In ratiometric converter applications, the magnitude of the reference voltage is a factor in both the output of the source transducer and the output of the A/D converter and therefore cancels out in the final digital output code. The ADC0805 is specified particularly for use in ratiometric applications with no adjustments required. In absolute conversion applications, both the initial value and the temperature stability of the reference voltage are important factors in the accuracy of the A/D converter. For $\mathrm{V}_{\mathrm{REF}} / 2$ voltages of $2.4 \mathrm{~V}_{\mathrm{DC}}$ nominal value, initial errors of $\pm 10$ $\mathrm{mV}_{\mathrm{DC}}$ will cause conversion errors of $\pm 1$ LSB due to the gain of 2 of the $\mathrm{V}_{\text {REF }} / 2$ input. In reduced span applications, the initial value and the stability of the $\mathrm{V}_{\mathrm{REF}} / 2$ input voltage become even more important. For example, if the span is reduced to 2.5 V , the analog input LSB voltage value is correspondingly reduced from $20 \mathrm{mV}(5 \mathrm{~V}$ span) to 10 mV and 1 LSB at the $\mathrm{V}_{\mathrm{REF}} / 2$ input becomes 5 mV . As can be seen, this reduces the allowed initial tolerance of the reference voltage and requires correspondingly less absolute change with temperature variations. Note that spans smaller than 2.5 V place even tighter requirements on the initial accuracy and stability of the reference source.
In general, the magnitude of the reference voltage will require an initial adjustment. Errors due to an improper value of reference voltage appear as full-scale errors in the A/D transfer function. IC voltage regulators may be used for references if the ambient temperature changes are not excessive. The LM336B 2.5V IC reference diode (from National Semiconductor) has a temperature stability of 1.8 mV typ ( 6 mV max ) over $0^{\circ} \mathrm{C} \leq \mathrm{T}_{\mathrm{A}} \leq+70^{\circ} \mathrm{C}$. Other temperature range parts are also available.

### 2.5 Errors and Reference Voltage Adjustments

2.5.1 Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, $\mathrm{V}_{I N(M I N)}$, is not ground, a zero offset can be done. The converter can be made to output 00000000 digital code for this minimum input voltage by biasing the $A / D V_{I N}(-)$ input at this $V_{I N(M I N)}$ value (see Applications section). This utilizes the differential mode operation of the A/D.
The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the $\mathrm{V}_{\mathrm{IN}}(-)$ input and applying a small magnitude positive voltage to the $\mathrm{V}_{\mathrm{IN}}(+)$ input. Zero error is the difference between the actual DC input voltage that is necessary to just cause an output digital code transition from 00000000 to 00000001 and the ideal $1 / 2$ LSB value $\left(1 / 2 \mathrm{LSB}=9.8 \mathrm{mV}\right.$ for $\left.\mathrm{V}_{\text {REF }} / 2=2.500 \mathrm{~V}_{\mathrm{DC}}\right)$.

### 2.5.2 Full-Scale

The full-scale adjustment can be made by applying a differential input voltage that is $11 / 2$ LSB less than the desired analog full-scale voltage range and then adjusting the magnitude of the $\mathrm{V}_{\text {REF }} / 2$ input (pin 9 or the $\mathrm{V}_{\mathrm{CC}}$ supply if pin 9 is not used) for a digital output code that is just changing from 11111110 to 11111111.

## Functional Description (Continued)

### 2.5.3 Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal that does not go to ground) this new zero reference should be properly adjusted first. A $\mathrm{V}_{\mathrm{IN}}(+)$ voltage that equals this desired zero reference plus $1 / 2$ LSB (where the LSB is calculated for the desired analog span, $1 \mathrm{LSB}=$ ana$\log$ span/256) is applied to pin 6 and the zero reference voltage at pin 7 should then be adjusted to just obtain the $00_{\text {HEX }}$ to $01_{\text {HEX }}$ code transition.
The full-scale adjustment should then be made (with the proper $\mathrm{V}_{\mathrm{IN}}(-)$ voltage applied) by forcing a voltage to the $\mathrm{V}_{\mathrm{IN}}(+)$ input which is given by:

$$
\mathrm{V}_{\mathrm{IN}}(+) \text { fs adj }=\mathrm{V}_{\mathrm{MAX}}-1.5\left[\frac{\left(\mathrm{~V}_{\mathrm{MAX}}-\mathrm{V}_{\mathrm{MIN}}\right)}{256}\right]
$$

where:
$\mathrm{V}_{\mathrm{MAX}}=$ The high end of the analog input range and
$\mathrm{V}_{\text {MIN }}=$ the low end (the offset zero) of the analog range. (Both are ground referenced.)
The $\mathrm{V}_{\mathrm{REF}} / 2$ (or $\mathrm{V}_{\mathrm{CC}}$ ) voltage is then adjusted to provide a code change from $\mathrm{FE}_{\text {HEX }}$ to $\mathrm{FF}_{\text {HEX }}$. This completes the adjustment procedure.

### 2.6 Clocking Option

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The CLK IN (pin 4) makes use of a Schmitt trigger as shown in Figure 6.


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FIGURE 6. Self-Clocking the A/D
Heavy capacitive or DC loading of the clock R pin should be avoided as this will disturb normal converter operation. Loads less than 50 pF , such as driving up to 7 A/D converter clock inputs from a single clock $R$ pin of 1 converter, are allowed. For larger clock line loading, a CMOS or low power TTL buffer or PNP input logic should be used to minimize the loading on the clock R pin (do not use a standard TTL buffer).

### 2.7 Restart During a Conversion

If the $A / D$ is restarted ( $\overline{C S}$ and $\overline{W R}$ go low and return high) during a conversion, the converter is reset and a new conversion is started. The output data latch is not updated if the
conversion in process is not allowed to be completed, therefore the data of the previous conversion remains in this latch. The INTR output simply remains at the " 1 " level.

### 2.8 Continuous Conversions

For operation in the free-running mode an initializing pulse should be used, following power-up, to ensure circuit operation. In this application, the $\overline{\mathrm{CS}}$ input is grounded and the $\overline{\mathrm{WR}}$ input is tied to the $\overline{\mathrm{INTR}}$ output. This $\overline{\mathrm{WR}}$ and $\overline{\mathrm{INTR}}$ node should be momentarily forced to logic low following a power-up cycle to guarantee operation.

### 2.9 Driving the Data Bus

This MOS A/D, like MOS microprocessors and memories, will require a bus driver when the total capacitance of the data bus gets large. Other circuitry, which is tied to the data bus, will add to the total capacitive loading, even in TRISTATE (high impedance mode). Backplane bussing also greatly adds to the stray capacitance of the data bus.
There are some alternatives available to the designer to handle this problem. Basically, the capacitive loading of the data bus slows down the response time, even though DC specifications are still met. For systems operating with a relatively slow CPU clock frequency, more time is available in which to establish proper logic levels on the bus and therefore higher capacitive loads can be driven (see typical characteristics curves).
At higher CPU clock frequencies time can be extended for I/O reads (and/or writes) by inserting wait states (8080) or using clock extending circuits (6800).
Finally, if time is short and capacitive loading is high, external bus drivers must be used. These can be TRI-STATE buffers (low power Schottky such as the DM74LS240 series is recommended) or special higher drive current products which are designed as bus drivers. High current bipolar bus drivers with PNP inputs are recommended.

### 2.10 Power Supplies

Noise spikes on the $\mathrm{V}_{\mathrm{CC}}$ supply line can cause conversion errors as the comparator will respond to this noise. A low inductance tantalum filter capacitor should be used close to the converter $\mathrm{V}_{\mathrm{CC}}$ pin and values of $1 \mu \mathrm{~F}$ or greater are recommended. If an unregulated voltage is available in the system, a separate LM340LAZ-5.0, TO-92, 5 V voltage regulator for the converter (and other analog circuitry) will greatly reduce digital noise on the $\mathrm{V}_{\mathrm{CC}}$ supply.

### 2.11 Wiring and Hook-Up Precautions

Standard digital wire wrap sockets are not satisfactory for breadboarding this A/D converter. Sockets on PC boards can be used and all logic signal wires and leads should be grouped and kept as far away as possible from the analog signal leads. Exposed leads to the analog inputs can cause undesired digital noise and hum pickup, therefore shielded leads may be necessary in many applications.

## Functional Description (Continued)

A single point analog ground that is separate from the logic ground points should be used. The power supply bypass capacitor and the self-clocking capacitor (if used) should both be returned to digital ground. Any $\mathrm{V}_{\mathrm{REF}} / 2$ bypass capacitors, analog input filter capacitors, or input signal shielding should be returned to the analog ground point. A test for proper grounding is to measure the zero error of the A/D converter. Zero errors in excess of $1 / 4$ LSB can usually be traced to improper board layout and wiring (see section 2.5.1 for measuring the zero error).

### 3.0 TESTING THE A/D CONVERTER

There are many degrees of complexity associated with testing an A/D converter. One of the simplest tests is to apply a known analog input voltage to the converter and use LEDs to display the resulting digital output code as shown in Figure 7 .
For ease of testing, the $\mathrm{V}_{\text {REF }} / 2$ (pin 9) should be supplied with $2.560 \mathrm{~V}_{\mathrm{DC}}$ and a $\mathrm{V}_{\mathrm{CC}}$ supply voltage of $5.12 \mathrm{~V}_{\mathrm{DC}}$ should be used. This provides an LSB value of 20 mV .
If a full-scale adjustment is to be made, an analog input voltage of $5.090 \mathrm{~V}_{\mathrm{DC}}(5.120-11 / 2 \mathrm{LSB})$ should be applied to the $\mathrm{V}_{\mathrm{IN}}(+)$ pin with the $\mathrm{V}_{\mathrm{IN}}(-)$ pin grounded. The value of the $\mathrm{V}_{\text {REF }} / 2$ input voltage should then be adjusted until the digital output code is just changing from 11111110 to 1111 1111. This value of $\mathrm{V}_{\text {REF }} / 2$ should then be used for all the tests.
The digital output LED display can be decoded by dividing the 8 bits into 2 hex characters, the 4 most significant (MS) and the 4 least significant (LS). Table I shows the fractional binary equivalent of these two 4-bit groups. By adding the voltages obtained from the "VMS" and "VLS" columns in Table I, the nominal value of the digital display (when


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FIGURE 7. Basic A/D Tester
$\mathrm{V}_{\text {REF }} / 2=2.560 \mathrm{~V}$ ) can be determined. For example, for an output LED display of 10110110 or B6 (in hex), the voltage values from the table are $3.520+0.120$ or $3.640 \mathrm{~V}_{\mathrm{DC}}$. These voltage values represent the center-values of a perfect A/D converter. The effects of quantization error have to be accounted for in the interpretation of the test results.
For a higher speed test system, or to obtain plotted data, a digital-to-analog converter is needed for the test set-up. An accurate 10-bit DAC can serve as the precision voltage source for the A/D. Errors of the A/D under test can be expressed as either analog voltages or differences in 2 digital words.
A basic A/D tester that uses a DAC and provides the error as an analog output voltage is shown in Figure 8. The 2 op amps can be eliminated if a lab DVM with a numerical subtraction feature is available to read the difference voltage, "A-C", directly. The analog input voltage can be supplied by a low frequency ramp generator and an X-Y plotter can be used to provide analog error ( Y axis) versus analog input ( X axis).
For operation with a microprocessor or a computer-based test system, it is more convenient to present the errors digitally. This can be done with the circuit of Figure 9, where the output code transitions can be detected as the 10-bit DAC is incremented. This provides $1 / 4$ LSB steps for the 8 -bit A/D under test. If the results of this test are automatically plotted with the analog input on the X axis and the error (in LSB's) as the $Y$ axis, a useful transfer function of the A/D under test results. For acceptance testing, the plot is not necessary and the testing speed can be increased by establishing internal limits on the allowed error for each code.

### 4.0 MICROPROCESSOR INTERFACING

To dicuss the interface with 8080A and 6800 microprocessors, a common sample subroutine structure is used. The microprocessor starts the A/D, reads and stores the results of 16 successive conversions, then returns to the user's program. The 16 data bytes are stored in 16 successive memory locations. All Data and Addresses will be given in hexadecimal form. Software and hardware details are provided separately for each type of microprocessor.

### 4.1 Interfacing 8080 Microprocessor Derivatives (8048, 8085)

This converter has been designed to directly interface with derivatives of the 8080 microprocessor. The A/D can be mapped into memory space (using standard memory address decoding for $\overline{\mathrm{CS}}$ and the MEMR and MEMW strobes) or it can be controlled as an I/O device by using the $\overline{1 / O R}$ and I/O W strobes and decoding the address bits AO $\rightarrow$ A7 (or address bits A8 $\rightarrow$ A15 as they will contain the same 8 -bit address information) to obtain the $\overline{\mathrm{CS}}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8-bit address decoder but the data can only be input to the accumulator. To make use of the additional memory reference instructions, the A/D should be mapped into memory space. An example of an A/D in I/O space is shown in Figure 10.

Functional Description (Continued)


FIGURE 8. A/D Tester with Analog Error Output


FIGURE 9. Basic "Digital" A/D Tester

TABLE I. DECODING THE DIGITAL OUTPUT LEDs

| HEX |  | BIN | RY |  |  |  | FRA | TIONAL | INARY | VALUE | OR |  | $\begin{array}{r} \text { OUTPUT } \\ \text { CENTER } \\ \mathrm{w} \\ \mathrm{~V}_{\text {REF }} / 2= \end{array}$ | OLTAGE <br> VALUES <br> H <br> $560 \mathrm{~V}_{\mathrm{DC}}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  |  |  | MS | ROUP |  |  |  | ROUP |  | VMS GROUP* | VLS GROUP* |
| F |  |  |  | 1 |  |  |  | 15/16 |  |  |  | 15/256 | 4.800 | 0.300 |
| E | 1 | 1 | 1 | 0 |  |  | 7/8 |  |  |  | 7/128 |  | 4.480 | 0.280 |
| D | 1 | 1 | 0 | 1 |  |  |  | 13/16 |  |  |  | 13/256 | 4.160 | 0.260 |
| C | 1 | 1 | 0 | 0 |  | 3/4 |  |  |  | 3/64 |  |  | 3.840 | 0.240 |
| B | 1 | 0 | 1 | 1 |  |  |  | 11/16 |  |  |  | 11/256 | 3.520 | 0.220 |
| A | 1 | 0 | 1 | 0 |  |  | 5/8 |  |  |  | 5/128 |  | 3.200 | 0.200 |
| 9 | 1 | 0 | 0 | 1 |  |  |  | 9/16 |  |  |  | 9/256 | 2/880 | 0.180 |
| 8 | 1 | 0 | 0 | 0 | 1/2 |  |  |  | 1/32 |  |  |  | 2/560 | 0.160 |
| 7 | 0 | 1 | 1 | 1 |  |  |  | 7/16 |  |  |  | 7/256 | 2.240 | 0.140 |
| 6 | 0 | 1 | 1 | 0 |  |  | 3/8 |  |  |  | 3/128 |  | 1.920 | 0.120 |
| 5 | 0 | 1 | 0 | 1 |  |  |  | 5/16 |  |  |  | 2/256 | 1.600 | 0.100 |
| 4 | 0 | 1 | 0 | 0 |  | 1/4 |  |  |  | 1/64 |  |  | 1/280 | 0.080 |
| 3 |  | 0 | 1 | 1 |  |  |  | 3/16 |  |  |  | 3/256 | 0.960 | 0.060 |
| 2 |  | 0 | 1 | 0 |  |  | 1/8 |  |  |  | 1/128 |  | 0.640 | 0.040 |
| 1 |  | 0 | 0 | 1 |  |  |  | 1/16 |  |  |  | 1/256 | 0.320 | 0.020 |
| 0 |  | 0 | 0 | 0 |  |  |  |  |  |  |  |  | 0 | 0 |
| *Display Output $=$ VMS Group + VLS Group |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

Functional Description (Continued)


Note 1: *Pin numbers for the DP8228 system controller, others are INS8080A.
Note 2: Pin 23 of the INS8228 must be tied to +12 V through a $1 \mathrm{k} \Omega$ resistor to generate the RST 7 instruction when an interrupt is acknowledged as required by the accompanying sample program.

FIGURE 10. ADC0801-INS8080A CPU Interface
SAMPLE PROGRAM FOR FIGURE 10 ADC0801-INS8080A CPU INTERFACE


Note 1: The stack pointer must be dimensioned because a RST 7 instruction pushes the PC onto the stack.
Note 2: All address used were arbitrarily chosen.

## Functional Description (Continued)

The standard control bus signals of the $8080 \overline{\mathrm{CS}}, \overline{\mathrm{RD}}$ and $\overline{\mathrm{WR}}$ ) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and outputting the data onto the data bus. A bus driver should be used for larger microprocessor systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100 pF .

### 4.1.1 Sample 8080A CPU Interfacing Circuitry and Program

The following sample program and associated hardware shown in Figure 10 may be used to input data from the converter to the INS8080A CPU chip set (comprised of the INS8080A microprocessor, the INS8228 system controller and the INS8224 clock generator). For simplicity, the A/D is controlled as an I/O device, specifically an 8-bit bi-directional port located at an arbitrarily chosen port address, E0. The TRI-STATE output capability of the A/D eliminates the need for a peripheral interface device, however address decoding is still required to generate the appropriate $\overline{\mathrm{CS}}$ for the converter.

It is important to note that in systems where the A/D converter is 1 -of-8 or less I/O mapped devices, no address decoding circuitry is necessary. Each of the 8 address bits (A0 to A7) can be directly used as $\overline{\mathrm{CS}}$ inputs-one for each /O device.

### 4.1.2 INS8048 Interface

The INS8048 interface technique with the ADC0801 series (see Figure 11) is simpler than the 8080A CPU interface. There are 24 I/O lines and three test input lines in the 8048. With these extra I/O lines available, one of the I/O lines (bit 0 of port 1) is used as the chip select signal to the A/D, thus eliminating the use of an external address decoder. Bus control signals $\overline{\mathrm{RD}}, \overline{\mathrm{WR}}$ and $\overline{\mathrm{INT}}$ of the 8048 are tied directly to the A/D. The 16 converted data words are stored at onchip RAM locations from 20 to 2F (Hex). The $\overline{R D}$ and WR signals are generated by reading from and writing into a dummy address, respectively. A sample interface program is shown below.


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FIGURE 11. INS8048 Interface
SAMPLE PROGRAM FOR FIGURE 11 INS 8048 INTERFACE

| 0410 |  | JMP | 10 H | : Program starts at addr 10 |
| :---: | :---: | :---: | :---: | :---: |
|  |  | ORG | 3H |  |
| 0450 |  | JMP | 50 H | ; Interrupt jump vector |
|  |  | ORG | 10H | ; Main program |
| 99 FE |  | ANL | Pl, \#OFEH | ; Chip select |
| 81 |  | MOVX | A, @RI | ; Read in the lst data <br> ; to reset the intr |
| 8901 | START : | ORL | P1, \#1 | ; Set port pin high |
| B8 20 |  | MOV | R0, \#20H | ; Data address |
| B9 FF |  | MOV | R1, \#OFFH | ; Dummy address |
| BA 10 |  | MOV | R2, \#l0H | ; Counter for 16 bytes |
| 23 FF | AGAIN : | MOV | A, \#OFFH | ; Set ACC for intr loop |
| 99 FE |  | ANL | Pl, \#OFEH | ; Send CS (bit 0 of Pl) |
| 91 |  | MOVX | @Rl, A | ; Send WR out |
| 05 |  | EN | I | ; Enable interrupt |
| 9621 | L00P : | JNZ | LOOP | ; Wait for interrupt |
| EA 1B |  | DJNZ | R2, AGAIN | ; If 16 bytes are read |
| 00 |  | NOP |  | ; go touser's program |
| 00 |  | NOP |  |  |
|  |  | ORG | 50H |  |
| 81 | INDATA: | MOVX | A, @RI | ; Input data, CS still low |
| A0 |  | MOV | @RO, A | ; Store inmemory |
| 18 |  | INC | R0 | ; Increment storage counter |
| 8901 |  | ORL | Pl, \#l | ; Reset CS signal |
| 27 |  | CLR | A | ; Clear ACC to get out of |
| 93 |  | RETR |  | ; the interrupt loop |

## Functional Description (Continued)

### 4.2 Interfacing the Z-80

The Z-80 control bus is slightly different from that of the 8080. General $\overline{\mathrm{RD}}$ and $\overline{\mathrm{WR}}$ strobes are provided and separate memory request, MREQ, and I/O request, IORQ, signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{\mathrm{RD}}$ and $\overline{W R}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in Figure 13.


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FIGURE 13. Mapping the A/D as an I/O Device for Use with the Z-80 CPU
Additional I/O advantages exist as software DMA routines are available and use can be made of the output data transfer which exists on the upper 8 address lines (A8 to A15) during I/O input instructions. For example, MUX channel selection for the A/D can be accomplished with this operating mode.

### 4.3 Interfacing 6800 Microprocessor Derivatives

 (6502, etc.)The control bus for the 6800 microprocessor derivatives does not use the $\overline{\mathrm{RD}}$ and $\overline{\mathrm{WR}}$ strobe signals. Instead it employs a single $R / \bar{W}$ line and additional timing, if needed, can be derived fom the $\phi 2$ clock. All I/O devices are memory mapped in the 6800 system, and a special signal, VMA, indicates that the current address is valid. Figure 14 shows an interface schematic where the A/D is memory mapped in the 6800 system. For simplicity, the $\overline{C S}$ decoding is shown using $1 / 2$ DM8092. Note that in many 6800 systems, an al-
ready decoded $\overline{4 / 5}$ line is brought out to the common bus at pin 21 . This can be tied directly to the $\overline{C S}$ pin of the A/D, provided that no other devices are addressed at HX ADDR: 4 XXX or 5 XXX .
The following subroutine performs essentially the same function as in the case of the 8080A interface and it can be called from anywhere in the user's program.
In Figure 15 the ADC0801 series is interfaced to the M6800 microprocessor through (the arbitrarily chosen) Port B of the MC6820 or MC6821 Peripheral Interface Adapter, (PIA). Here the CS pin of the A/D is grounded since the PIA is already memory mapped in the M6800 system and no $\overline{\mathrm{CS}}$ decoding is necessary. Also notice that the A/D output data lines are connected to the microprocessor bus under program control through the PIA and therefore the A/D $\overline{\mathrm{RD}}$ pin can be grounded.
A sample interface program equivalent to the previous one is shown below Figure 15. The PIA Data and Control Registers of Port B are located at HEX addresses 8006 and 8007, respectively.

### 5.0 GENERAL APPLICATIONS

The following applications show some interesting uses for the A/D. The fact that one particular microprocessor is used is not meant to be restrictive. Each of these application circuits would have its counterpart using any microprocessor that is desired.
5.1 Multiple ADC0801 Series to MC6800 CPU Interface

To transfer analog data from several channels to a single microprocessor system, a multiple converter scheme presents several advantages over the conventional multiplexer single-converter approach. With the ADC0801 series, the differential inputs allow individual span adjustment for each channel. Furthermore, all analog input channels are sensed simultaneously, which essentially divides the microprocessor's total system servicing time by the number of channels, since all conversions occur simultaneously. This scheme is shown in Figure 16.


Functional Description (Continued)

| SAMPLE PROGRAM FOR FIGURE 14 ADC0801-MC6800 CPU INTERFACE |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0010 | DF 36 | DATAIN | STX | TEMP2 | ; Save contents of X |
| 0012 | CE 002 C |  | LDX | \#\$002C | ; Upon $\overline{I R Q}$ low CPU |
| 0015 | FFFFF8 |  | STX | \$FFF8 | ; jumps to 002C |
| 0018 | B7 5000 |  | STAA | \$5000 | ; Start ADC0801 |
| 001B | OE |  | CLI |  |  |
| 001C | 3E | CONVRT | WAI |  | ; Wait for interrupt |
| 001D | DE 34 |  | LDX | TEMPI |  |
| 001F | 8C 020 F |  | CPX | \#\$020F | ; Is final data stored? |
| 0022 | 2714 |  | BEQ | ENDP |  |
| 0024 | B7 5000 |  | STAA | \$5000 | ; Restarts ADC0801 |
| 0027 | 08 |  | INX |  |  |
| 0028 | DF 34 |  | STX | TEMPI |  |
| 002A | 20 FO |  | BRA | CONVRT |  |
| 002C | DE 34 | INTRPT | LDX | TEMPI |  |
| 002E | B6 5000 |  | LDAA | \$5000 | ; Read data |
| 0031 | A7 00 |  | STAA | X | ; Store it at X |
| 0033 | 3B |  | RTI |  |  |
| 0034 | 0200 | TEMPI | FDB | \$0200 | ; Starting address for <br> ; data storage |
| 0036 | 0000 | TEMP2 | FDB | \$0000 |  |
| 0038 | CE 0200 | ENDP | LDX | \#\$0200 | ; Reinitialize TEMP1 |
| 003B | DF 34 |  | STX | TEMPI |  |
| 003D | DE 36 |  | LDX | TEMP2 |  |
| 003F | 39 |  | RTS |  | ; Return from subroutine <br> ; Touser's program |



FIGURE 15. ADC0801-MC6820 PIA Interface
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## Functional Description (Continued)

SAMPLE PROGRAM FOR FIGURE 15 ADC0801-MC6820 PIA INTERFACE

| 0010 | CE 0038 | DATAIN | LDX | \#\$0038 | ; Upon $\overline{\text { IRQ }}$ low CPU |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0013 | FFFF F8 |  | STX | \$FFF8 | ; jumps to 0038 |
| 0016 | B6 8006 |  | LDAA | PIAORB | ; Clear possible $\overline{\text { IRQ flags }}$ |
| 0019 | 4 F |  | CLRA |  |  |
| 001A | B7 8007 |  | STAA | PIACRB |  |
| 001D | B7 8006 |  | STAA | PIAORB | ; Set Port B as input |
| 0020 | OE |  | CLI |  |  |
| 0021 | C6 34 |  | LDAB | \#\$34 |  |
| 0023 | 86 3D |  | LDAA | \#\$3D |  |
| 0025 | F7 8007 | CONVRT | STAB | PIACRB | ; Starts ADC0801 |
| 0028 | B7 8007 |  | STAA | PIACRB |  |
| 002B | 3E |  | WAI |  | ; Wait for interrupt |
| 002C | DE 40 |  | LDX | TEMP1 |  |
| 002E | 8C 02 0F |  | CPX | \#\$020F | ; Is final data stored? |
| 0031 | 27 0F |  | BEQ | ENDP |  |
| 0033 | 08 |  | INX |  |  |
| 0034 | DF 40 |  | STX | TEMP1 |  |
| 0036 | 20 ED |  | BRA | CONVRT |  |
| 0038 | DE 40 | INTRPT | LDX | TEMPI |  |
| 003A | B6 8006 |  | LDAA | PIAORB | ; Read data in |
| 003D | A7 00 |  | STAA | X | ; Store it at X |
| 003F | 3B |  | RTI |  |  |
| 0040 | 0200 | TEMPI | FDB | \$0200 | ; Starting address for <br> ; data storage |
| 0042 | CE 0200 | ENDP | LDX | \#\$0200 | ; Reinitialize TEMP1 |
| 0045 | DF 40 |  | STX | TEMP1 |  |
| 0047 | 39 |  | RTS |  | ; Return from subroutine |
|  |  | PIAORB | EQU | \$8006 | ; Touser's program |
|  |  | PIACRB | EQU | \$8007 |  |

The following schematic and sample subroutine (DATA IN) may be used to interface (up to) 8 ADC0801's directly to the MC6800 CPU. This scheme can easily be extended to allow the interface of more converters. In this configuration the converters are (arbitrarily) located at HEX address 5000 in the MC6800 memory space. To save components, the clock signal is derived from just one RC pair on the first converter. This output drives the other A/Ds.
All the converters are started simultaneously with a STORE instruction at HEX address 5000. Note that any other HEX address of the form 5XXX will be decoded by the circuit, pulling all the $\overline{\mathrm{CS}}$ inputs low. This can easily be avoided by using a more definitive address decoding scheme. All the interrupts are ORed together to insure that all A/Ds have completed their conversion before the microprocessor is interrupted.
The subroutine, DATA IN, may be called from anywhere in the user's program. Once called, this routine initializes the

CPU, starts all the converters simultaneously and waits for the interrupt signal. Upon receiving the interrupt, it reads the converters (from HEX addresses 5000 through 5007) and stores the data successively at (arbitrarily chosen) HEX addresses 0200 to 0207, before returning to the user's program. All CPU registers then recover the original data they had before servicing DATA IN.

### 5.2 Auto-Zeroed Differential Transducer Amplifier and A/D Converter

The differential inputs of the ADC0801 series eliminate the need to perform a differential to single ended conversion for a differential transducer. Thus, one op amp can be eliminated since the differential to single ended conversion is provided by the differential input of the ADC0801 series. In general, a transducer preamp is required to take advantage of the full $A / D$ converter input dynamic range.

Functional Description (Continued)


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FIGURE 16. Interfacing Multiple A/Ds in an MC6800 System
SAMPLE PROGRAM FOR FIGURE 16 INTERFACING MULTIPLE A/Ds IN AN MC6800 SYSTEM

| ADDRESS | HEX CODE |  | MNEMONICS |  | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0010 | DF 44 | DATAIN | STX | TEMP | ; Save Contents of X |
| 0012 | CE 00 2A |  | LDX | \#\$002A | ; Upon $\overline{I R Q}$ LOW CPU |
| 0015 | FF FF F8 |  | STX | \$FFF8 | ; Jumps to 002A |
| 0018 | B7 5000 |  | STAA | \$5000 | ; Starts all A/D's |
| 001B | OE |  | CLI |  |  |
| 001C | 3E |  | WAI |  | ; Wait for interrupt |
| 001D | CE 5000 |  | LDX | \#\$5000 |  |
| 0020 | DF 40 |  | STX | INDEXI | ; Reset both INDEX |
| 0022 | CE 0200 |  | LDX | \#\$0200 | ; 1 and 2 to starting |
| 0025 | DF 42 |  | STX | INDEX2 | ; addresses |
| 0027 | DE 44 |  | LDX | TEMP |  |
| 0029 | 39 |  | RTS |  | ; Return from subroutine |
| 002A | DE 40 | INTRPT | LDX | INDEX1 | ; INDEXI $\rightarrow$ X |
| 002C | A6 00 |  | LDAA | X | ; Read data in from A/D at X |
| 002E | 08 |  | INX |  | ; Increment $X$ by one |
| 002F | DF 40 |  | STX | INDEX1 | ; $\mathrm{X} \rightarrow$ INDEXI |
| 0031 | DE 42 |  | LDX | INDEX2 | ; INDEX2 $\rightarrow$ X |

## Functional Description (Continued)

| ADDRESS | HEX CODE |  | MNEMONICS |  | COMMENTS |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 0033 | A7 00 |  | STAA | X | ; Store data at X |
| 0035 | 8C 0207 |  | CPX | \#\$0207 | ; Have all A/D's been read? |
| 0038 | 2705 |  | BEQ | RETURN | ; Yes: branch to RETURN |
| 003A | 08 |  | INX |  | ; No: increment X by one |
| 003B | DF 42 |  | STX | INDEX2 | ; $\mathrm{X} \rightarrow$ INDEX2 |
| 003D | 20 EB |  | BRA | INTRPT | ; Branch to 002A |
| 003F | 3B | RETURN | RTI |  |  |
| 0040 | 5000 | INDEXI | FDB | \$5000 | ; Starting address for A/D |
| 0042 | 0200 | INDEX2 | FDB | \$0200 | ; Starting address for data storage |
| 0044 | 0000 | TEMP | FDB | \$0000 |  |

Note 1: In order for the microprocessor to service subroutines and interrupts, the stack pointer must be dimensioned in the user's program

For amplification of DC input signals, a major system error is the input offset voltage of the amplifiers used for the preamp. Figure 17 is a gain of 100 differential preamp whose offset voltage errors will be cancelled by a zeroing subroutine which is performed by the INS8080A microprocessor system. The total allowable input offset voltage error for this preamp is only $50 \mu \mathrm{~V}$ for $1 / 4$ LSB error. This would obviously require very precise amplifiers. The expression for the differential output voltage of the preamp is:

$$
\underbrace{\mathrm{V}_{\mathrm{O}}=\left[\mathrm{V}_{\mathrm{IN}( }(+)-\mathrm{V}_{\mathrm{IN}( }(-)\right]}_{\text {SIGNAL }}[\underbrace{\left.1+\frac{2 R 2}{R 1}\right]}_{\text {GAIN }}+
$$

where $\mathrm{I}_{\mathrm{X}}$ is the current through resistor RX. All of the offset error terms can be cancelled by making $\pm I_{X} R_{X}=V_{O S 1}+$ $\mathrm{V}_{\text {OS3 }}-\mathrm{V}_{\text {OS2 }}$. This is the principle of this auto-zeroing scheme.
The INS8080A uses the 3 I/O ports of an INS 8255 Programable Peripheral Interface (PPI) to control the auto zeroing and input data from the ADC0801 as shown in Figure 18. The PPI is programmed for basic I/O operation (mode 0 ) with Port A being an input port and Ports B and C being output ports. Two bits of Port C are used to alternately open or close the 2 switches at the input of the preamp. Switch

SW1 is closed to force the preamp's differential input to be zero during the zeroing subroutine and then opened and SW2 is then closed for conversion of the actual differential input signal. Using 2 switches in this manner eliminates concern for the ON resistance of the switches as they must conduct only the input bias current of the input amplifiers.
Output Port B is used as a successive approximation register by the 8080 and the binary scaled resistors in series with each output bit create a D/A converter. During the zeroing subroutine, the voltage at $\mathrm{V}_{\mathrm{x}}$ increases or decreases as required to make the differential output voltage equal to zero. This is accomplished by ensuring that the voltage at the output of A 1 is approximately 2.5 V so that a logic " 1 " ( 5 V ) on any output of Port $B$ will source current into node $V_{X}$ thus raising the voltage at $V_{X}$ and making the output differential more negative. Conversely, a logic " 0 " ( 0 V ) will pull current out of node $V_{X}$ and decrease the voltage, causing the differential output to become more positive. For the resistor values shown, $V_{X}$ can move $\pm 12 \mathrm{mV}$ with a resolution of 50 $\mu \mathrm{V}$, which will null the offset error term to $1 / 4$ LSB of fullscale for the ADC0801. It is important that the voltage levels that drive the auto-zero resistors be constant. Also, for symmetry, a logic swing of $O \mathrm{~V}$ to 5 V is convenient. To achieve this, a CMOS buffer is used for the logic output signals of Port B and this CMOS package is powered with a stable 5 V source. Buffer amplifier A1 is necessary so that it can source or sink the D/A output current.

Functional Description (Continued)


Note 1: R2 = 49.5 R1
Note 2: Switches are LMC13334 CMOS analog switches.
Note 3: The 9 resistors used in the auto-zero section can be $\pm 5 \%$ tolerance.
FIGURE 17. Gain of 100 Differential Transducer Preamp


TL/H/5671-27 FIGURE 18. Microprocessor Interface Circuitry for Differential Preamp

A flow chart for the zeroing subroutine is shown in Figure 19. It must be noted that the ADC0801 series will output an all zero code when it converts a negative input $\left[\mathrm{V}_{\text {IN }}(-) \geq\right.$ $\mathrm{V}_{\mathrm{IN}}(+)$. Also, a logic inversion exists as all of the I/O ports are buffered with inverting gates.
Basically, if the data read is zero, the differential output voltage is negative, so a bit in Port $B$ is cleared to pull $V_{X}$ more negative which will make the output more positive for the next conversion. If the data read is not zero, the output voltage is positive so a bit in Port $B$ is set to make $V_{X}$ more positive and the output more negative. This continues for 8 approximations and the differential output eventually converges to within 5 mV of zero.
The actual program is given in Figure 20. All addresses used are compatible with the BLC $80 / 10$ microcomputer system. In particular:

Port A and the ADC0801 are at port address E4
Port B is at port address E5
Port C is at port address E6
PPI control word port is at port address E7
Program Counter automatically goes to ADDR:3C3D upon acknowledgement of an interrupt from the ADC0801
5.3 Multiple A/D Converters in a Z-80 Interrupt Driven Mode

In data acquisition systems where more than one A/D converter (or other peripheral device) will be interrupting program execution of a microprocessor, there is obviously a need for the CPU to determine which device requires servicing. Figure 21 and the accompanying software is a method of determining which of 7 ADC0801 converters has completed a conversion (INTR asserted) and is requesting an interrupt. This circuit allows starting the A/D converters in any sequence, but will input and store valid data from the converters with a priority sequence of A/D 1 being read first, A/D 2 second, etc., through A/D 7 which would have the lowest priority for data being read. Only the converters whose INT is asserted will be read.
The key to decoding circuitry is the DM74LS373, 8-bit D type flip-flop. When the Z-80 acknowledges the interrupt, the program is vectored to a data input Z-80 subroutine. This subroutine will read a peripheral status word from the DM74LS373 which contains the logic state of the INTR outputs of all the converters. Each converter which initiates an interrupt will place a logic " 0 " in a unique bit position in the status word and the subroutine will determine the identity of the converter and execute a data read. An identifier word (which indicates which A/D the data came from) is stored in the next sequential memory location above the location of the data so the program can keep track of the identity of the data entered.


FIGURE 19. Flow Chart for Auto-Zero Routine



| Ordering Information |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: |
| TEMP RANGE |  | $0^{\circ} \mathrm{C} \mathrm{TO} 70^{\circ} \mathrm{C}$ | $0^{\circ} \mathrm{CTO} 70^{\circ} \mathrm{C}$ | $0^{\circ} \mathrm{CTO} 70^{\circ} \mathrm{C}$ | $-40^{\circ} \mathrm{C} \mathrm{TO}+85^{\circ} \mathrm{C}$ |
|  |  |  |  |  | ADC0801LCN |
|  | Adjusted |  |  |  |  |
| ERROR | $\pm 1 / 2 \text { Bit }$ | ADC0802LCWM | ADC0802LCV |  | ADC0802LCN |
|  | $\pm 1 / 2 \mathrm{Bit}$ <br> Adjusted | ADC0803LCWM | ADC0803LCV |  | ADC0803LCN |
|  | $\pm 1 \mathrm{Bit}$ <br> Unadjusted | ADC0804LCWM | ADC0804LCV | ADC0804LCN | ADC0805LCN |
| PACKAGE OUTLINE |  | M20B-Small Outline | V20A-Chip Carrier | N20A-Molded DIP |  |


| TEMP RANGE |  | $\mathbf{- 4 0}{ }^{\circ} \mathbf{C} \mathbf{~ T O}+\mathbf{8 5}{ }^{\circ} \mathbf{C}$ | $-\mathbf{5 5}{ }^{\circ} \mathbf{C}$ TO $+\mathbf{1 2 5}{ }^{\circ} \mathbf{C}$ |
| :---: | :---: | :---: | :---: |
| ERROR | $\pm 1 / 4$ Bit Adjusted | ADC0801LCJ | ADC0801LJ |
|  | $\pm 1 / 2$ Bit Unadjusted | ADC0802LCJ | ADC0802LJ, |
|  | $\pm 1 / 2$ Bit Adjusted | ADC0803LCJ | ADC0802LJ/883 |
|  | $\pm 1$ Bit Unadjusted | ADC0804LCJ |  |
| PACKAGE OUTLINE |  | J20A—Cavity DIP | J20A—Cavity DIP |

## Connection Diagrams

ADC080X
Dual-In-Line and Small Outline (SO) Packages


ADC080X
Molded Chip Carrier (PCC) Package


See Ordering Information


Physical Dimensions inches (millimeters)


## Physical Dimensions inches (millimeters) (Continued)


ADC0801/ADC0802/ADC0803/ADC0804/ADC0805

Physical Dimensions inches (millimeters) (Continued)


Molded Chip Carrier Package (V) Order Number ADC0802LCV, ADC0803LCV or ADC0804LCV NS Package Number V20A

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